

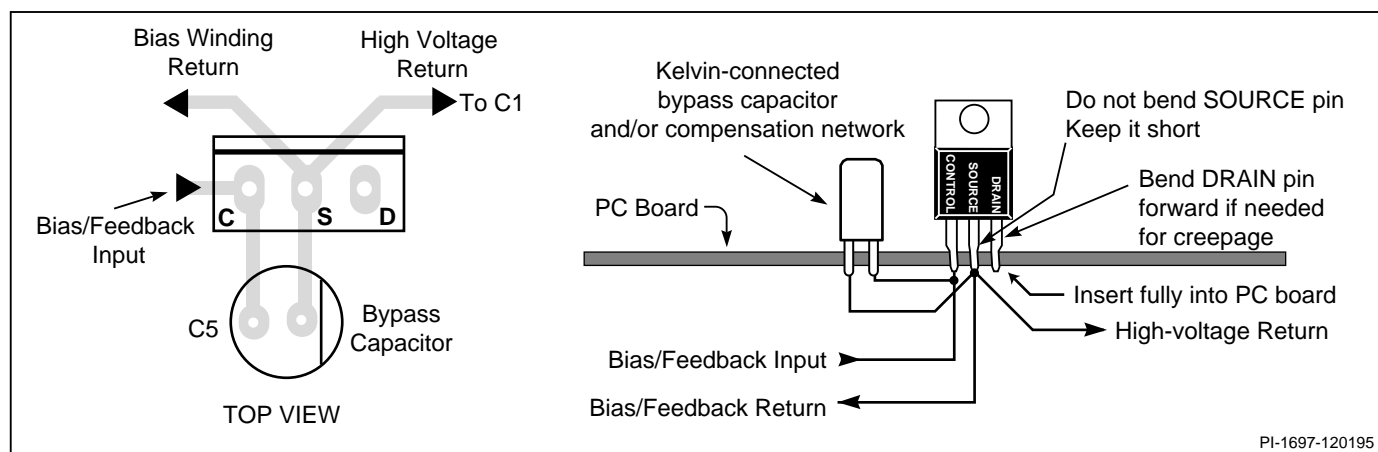
4. PC Layout

4.1 Single Point Ground/Kelvin Source Pin Connections

Figure 4 shows how auto-restart/compensation capacitor C5 must be connected to the Source pin using a single point ground or Kelvin connection. Proper layout prevents shutdown at turn on or instability due to high Source pin switching currents. High voltage return to input capacitor C1 must be connected directly to the Source pad with a separate trace **and must not share the**

C5 trace. Bias/feedback return should also be connected directly to the Source pad with a separate trace as shown.

The Source pin must be kept as short as possible. Do not bend or extend the Source pin. Insert *TOPSwitch* fully into the PC board as shown. Extend and bend the Drain pin if additional creepage distance on the PC board is necessary.



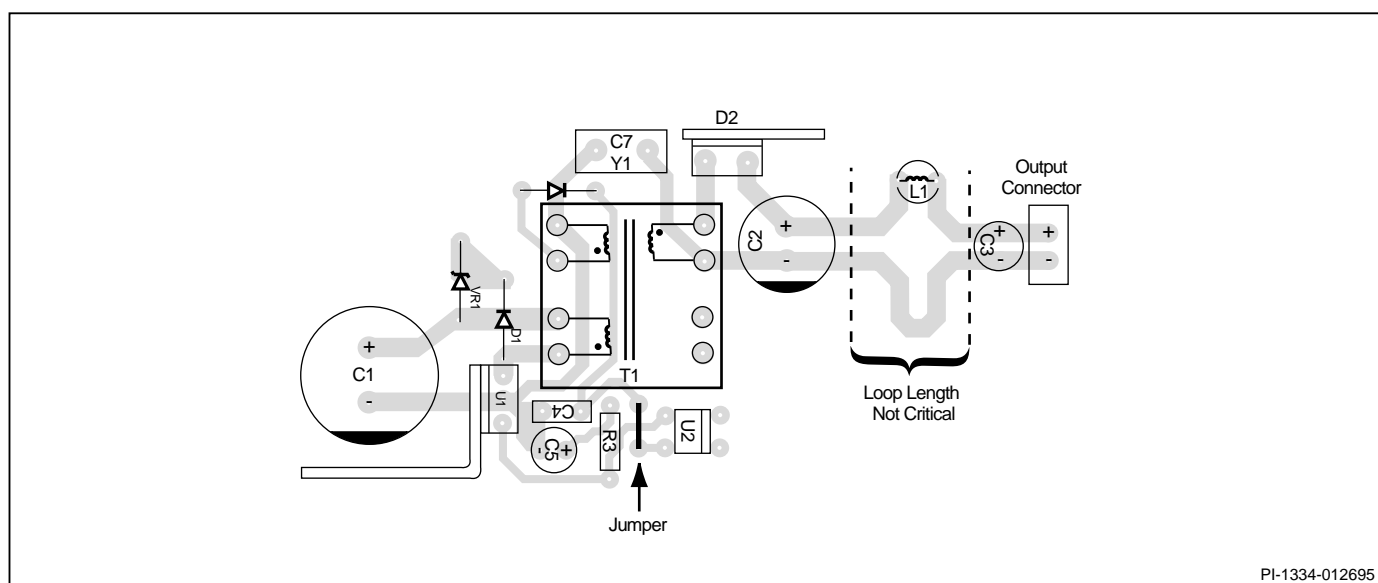
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Figure 4. Recommended TOPSwitch Layout.

4.2 Ideal Component Placement

Figure 5 shows ideal component placement and single sided PC trace connections for all critical power and EMI components with the ST204A schematic (Figure 3) used for reference.

A checklist is provided on the next page which is useful for uncovering potential PC layout related problems in any TOPSwitch power supply.



PI-1334-012695

Figure 5. Ideal Placement for Critical Components.

4.3 PC Layout Checklist:

- 1) *TOPSwitch* (U1), C1, and Transformer T1 primary pins should be very close together to minimize PC trace length and loop area. The traces connecting these components have fast switching currents which cause common mode EMI emissions. Note *TOPSwitch* alignment and right angle heat sink.
- 2) D1, VR1, and Transformer T1 primary pins should be very close together to minimize PC trace length and loop area. Traces connecting these components have fast switching currents which cause common mode EMI emissions.
- 3) *TOPSwitch* Drain connection to T1 primary pins and clamp diode D1 must be very short because, in addition to fast switching currents, this trace also has high switching voltage which causes additional common mode EMI emissions.
- 4) *TOPSwitch* Source pin should connect directly to C1 with no other traces connected to this trace segment.
- 5) Y1-capacitor C7 should connect directly to the transformer T1 primary bias winding return and secondary output winding return pins with short, wide traces.
- 6) Transformer T1 primary bias winding return should be connected directly to *TOPSwitch* Source pin. No other components should be connected to this trace segment because lightning surge test voltages induce noise voltage drops.
- 7) Bias diode D3 should be as close as possible to transformer T1 bias winding pins. This placement minimizes anode trace length (which has high switching voltages) and maximizes length of the relatively quiet cathode trace.
- 8) Cathode of D3 should connect directly to C4. No other components should be connected to this trace segment because lightning surge voltages and rectification current will induce noise voltage drops. C4 should then be connected through a PC trace and top side wire jumper to optocoupler U2.
- 9) Capacitor C4 should be connected directly to *TOPSwitch* Source pin with no other traces connected to this trace segment. No other components should be connected to this trace segment because lightning surge test voltages will induce noise voltage drops.
- 10) Capacitor C5 should be connected directly to *TOPSwitch* Source pin with no other traces connected to this trace segment. No other components should be connected to this trace segment because lightning surge test voltages will induce noise voltage drops.
- 11) Output rectifier D2, C2, and Transformer secondary pins should be very close together to minimize PC trace length and loop area. Traces connecting these components have fast switching currents which cause common mode EMI emissions. PC traces should be wide because peak currents are much higher than DC load current.
- 12) C3 should be close to the output connector and directly across the traces connecting to the output connector to minimize output switching noise. Note that the PC traces run right through the capacitor lead pads and that no additional PC traces have been placed in series with C3. Note also that PC traces in series with L1 and the PC trace connecting C2 and C3 can be narrower and longer because current flow is essentially DC.
- 13) Heat sinks should be either connected only to *TOPSwitch* tab or completely isolated from both *TOPSwitch* tab and circuit. If the heat sink is connected elsewhere in circuit but isolated from *TOPSwitch* tab, capacitance between *TOPSwitch* tab and heat sink can resonate with circuit inductance causing high frequency ringing currents which may trigger *TOPSwitch* shutdown latch.